Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A method of supporting memory addresses with holes, the method comprising the computer implemented steps of:

virtualizing a first physical address range allocated for system memory for an operating system run by a processor configured to support logical partitioning to produce a first logical address range;

virtualizing a second physical address range allocated for system memory for the operating system to produce a second logical address range, wherein the first physical address range and the second physical address range are non-contiguous and the first logical address range and the second logical address range are contiguous; and

virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range, wherein a lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address ranges.

2. (Original) The method of claim 1, wherein the steps of virtualizing the first physical address range, the second physical address range, and the memory mapped input/output physical address range comprises maintaining a mapping table that defines physical addresses and corresponding logical addresses.

3. (Original) The method of claim 2, wherein maintaining the mapping table further comprises maintaining the mapping table in a physical address space allocated to one of the first and second physical address ranges, and wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges.

4. (Original) The method of claim 1, wherein the third logical address range is non-contiguous with the first logical address range and the second logical address range.

5. (Original) The method of claim 1, further comprising:

allocating a portion of at least one of the first physical address range and the second physical address range for a logical partitioning management software layer.

6. (Original) The method of claim 1, wherein the memory mapped input/output physical address range is allocated for cache inhibited addresses.

7. (Previously presented) A computer program product that is stored in a computer readable medium for virtualizing non-contiguous physical memory ranges into a contiguous logical address range, the computer program product comprising:

instructions for virtualizing a first range of contiguous physical addresses, which are allocated for system memory for an operating system run by a processor configured to support logical partitioning, to produce a first range of contiguous logical addresses;

instructions for virtualizing a second range of contiguous physical addresses, which are allocated for system memory for the operating system, to produce a second range of contiguous logical addresses, the first range of contiguous physical addresses and the second range of contiguous physical addresses being non-contiguous, the first range of contiguous logical addresses and the second range of contiguous logical addresses being contiguous and forming a combined range of contiguous logical addresses; and

instructions for virtualizing a third range of contiguous physical addresses, which is allocated for memory mapped input/output, that is intermediate to the first range of contiguous physical addresses and the second range of contiguous physical addresses to produce a third range of contiguous logical addresses, a lowermost logical address of the third range of contiguous logical addresses exceeding an uppermost logical address of the combined range of contiguous logical addresses.

8. (Previously presented) The computer program product of claim 7, further comprising instructions for maintaining a mapping table that defines physical addresses and their corresponding logical addresses.

9. (Previously presented) The computer program product of claim 8, wherein the mapping table is maintained in at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses.

10. (Previously presented) The computer program product of claim 7, further comprising instructions for converting a logical physical address into a corresponding physical address.

11. (Previously presented) The computer program product of claim 7, further comprising:

instructions for converting a logical physical address into a corresponding physical address; and

the instructions for converting a logical physical address into a corresponding physical address being maintained in at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses.

12. (Previously presented) The computer program product of claim 7, wherein the third range of contiguous logical addresses and the combined range of contiguous logical addresses are non-contiguous.

13. (Previously presented) The computer program product of claim 12, further comprising:

instructions for allocating a portion of at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses for a logical partitioning management software layer.

14. (Previously presented) The computer program product of claim 7, wherein the third range of contiguous physical addresses is allocated for cache inhibited memory mapped input/output addresses.

15. (Previously presented) A data processing system for supporting non-contiguous system memory ranges, comprising:

a memory that contains a first range of contiguous physical addresses allocated for system memory, a second range of contiguous physical addresses allocated for system memory, and a third range of contiguous physical addresses allocated for memory-mapped input/output, the third range of contiguous physical addresses intermediate to the first range of contiguous physical addresses and the second range of contiguous physical memory addresses;

the first range of contiguous physical addresses and the second range of contiguous physical addresses being non-contiguous;

a processor for virtualizing the first range of contiguous physical addresses to produce a first range of contiguous logical addresses;

the processor for virtualizing the second range of contiguous physical addresses to produce a second range of contiguous logical addresses;

the first range of contiguous logical addresses and the second range of contiguous logical addresses being contiguous and forming a combined range of contiguous logical addresses; and

the processor for virtualizing the third range of contiguous physical addresses to produce a third range of contiguous logical addresses, a lowermost logical address of the third range of contiguous logical addresses exceeding an uppermost logical address of the combined range of contiguous logical addresses.

16. (Previously presented) The data processing system of claim 15, further comprising a data set, wherein the data set is a mapping table defining logical-to-physical memory address translations.

17. (Previously presented) The data processing system of claim 15, further comprising a set of instructions that is executed by the processor, wherein the set of instructions provides logical partitioning management.

18. (Previously presented) The data processing system of claim 15, further comprising a mapping table that defines logical-to-physical memory address translations, the mapping table maintained in the memory in at least one of the first and second ranges of contiguous physical addresses.

19. (Previously presented) The data processing system of claim 15, further comprising a set of instructions that is executed by the processor for virtualizing the first, second, and third ranges of contiguous physical addresses, wherein the set of instructions is maintained in the memory in at least one of the first and second ranges of contiguous physical addresses.

20. (Previously presented) The data processing system of claim 15, further comprising:

the combined range of contiguous logical addresses being non-contiguous with the third range of contiguous logical addresses.